CLAIMS

What is claimed is:

1. A printed circuit board (PCB) comprising:

a first signal routing layer formed on a first surface of the PCB;

at least one conductive plane and/or a second signal routing layer;

at least one padless via extending from the first signal routing layer to the at least one conductive plane and/or the second signal routing layer, the at least one padless via in electrical contact with the at least one conductive plane and/or a conductive trace on the second signal routing layer; and

a layer of solder mask material formed over the first signal routing layer, the layer of solder mask material having at least one opening to expose the at least one padless via.

2. The PCB of claim 1, wherein the second signal routing layer is an inner signal routing layer and the at least one padless via is a blind padless via extending from the first signal routing layer to the second signal routing layer.

3. The PCB of claim 1, further comprising a via plug formed within the padless via.

4. The PCB of claim 3, wherein the via plug is formed of an electrically conductive material.

5. The PCB of claim 1, further comprising a component attached to the PCB with a solder interconnection between a contact pad on a bottom surface of the component and the at least one padless via.

6. A printed circuit board (PCB) comprising:

a first signal routing layer formed on a first surface of the PCB;

at least one conductive plane and/or a second signal routing layer; and

an array of interconnections formed on the first surface of the PCB, the array of interconnections comprises at least one padless via extending from the first signal routing layer to the at least one conductive plane and/or the second signal routing layer, wherein the padless via is in electrical contact with the at least one conductive plane and/or a conductive trace on the second signal routing layer.

7. The PCB of claim 6, further comprising an electrically conductive via plug formed within the at least one padless via.

8. The PCB of claim 6, wherein the array of interconnections further comprises at least one contact pad electrically coupled with a conductive trace on the first signal routing layer, wherein the at least one contact pad has a diameter less than 18 mils.

9. The PCB of claim 6, further comprising at least two conductive traces formed on the first signal routing layer between the at least one padless via and an adjacent interconnection.

10. The PCB of claim 9, wherein the array of interconnections has an array pitch of 0.8 mm or less.

11. The PCB of claim 10, wherein the at least two conductive traces have a width of approximately 3 mils.

12. The PCB of claim 6, wherein the at least one padless via has a diameter of 12 mils or less.

13. A system comprising:

a printed circuit board (PCB) comprising a first signal routing layer formed on a first surface of the PCB, at least one conductive plane and/or a second signal routing layer, and an array of interconnections formed on the first surface of the PCB, wherein the array of interconnections comprises at least one padless via extending from the first signal routing layer to the at least one conductive plane and/or the second signal routing layer, the at least one padless via electrically connected to the at least one conductive plane and/or a conductive trace on the second signal routing layer; and

a component attached to the PCB by a plurality of solder ball interconnections between the array of interconnections formed on the first surface of the PCB and a corresponding array of contact pads disposed on a bottom surface of the electronic component.

14. The system of claim 13, wherein the component is a ball grid array (BGA) component having an array pitch less than 1.0 mm.

15. The system of claim 14, further comprising at least two conductive traces on the first signal routing layer routed between the at least one padless via and an adjacent interconnection.

16. The system of claim 15, wherein a width of the at least two conductive traces is approximately 3 mils.

17. The system of claim 13, wherein the at least one padless via has a diameter of 12 mils or less.

18. The system of claim 13, wherein the PCB is a motherboard and the component is a processor.

19. A method of fabricating a printed circuit board (PCB) comprising:

forming a first signal routing layer on a first surface of a printed circuit board (PCB); and

forming an array of interconnections on the first surface of the PCB, the array of interconnections comprising at least one padless via extending from the first signal routing layer to a conductive plane and/or a second signal routing layer, wherein the first padless via is in electrical contact with the conductive plane and/or a conductive trace on the second signal routing layer.

20. The method of claim 19, wherein the second signal routing layer is an inner signal routing layer and the at least one padless via is a blind via extending from the first signal routing layer to the second signal routing layer.

21. The method of claim 19, wherein forming an array of interconnections on the first surface of the PCB comprises forming an array of interconnections having an array pitch of 0.8 mm or less.

22. The method of claim 21, further comprising routing at least two conductive traces on the first signal routing layer between the at least one padless via and an adjacent interconnection.

23. The method of claim 19, further comprising forming a via plug within the at least one padless via.

24. The method of claim 19, wherein forming a via plug within the at least one padless via comprises overplating the at least one padless via to form a via plug of plating material.

25. The method of claim 19, wherein forming an array of interconnections on the first surface of the PCB comprises forming at least one contact pad on the first surface of the PCB adjacent to the at least one padless via, the at least one contact pad in electrical contact with a conductive trace on the first signal routing layer.

26. A method of attaching a component to a printed circuit board (PCB) comprising:

aligning solder balls attached to an array of contact pads on a bottom surface of the component with a corresponding array of interconnections formed on a first surface of the PCB, the array of interconnections comprising at least one padless via extending from a first signal routing layer on the first surface of the PCB to a conductive plane and/or a second signal routing layer within the PCB, wherein the at least one padless via is in electrical contact with the conductive plane and/or a conductive trace on the second signal routing layer; and

reflowing the solder balls to electrically connect the array of contact pads to the corresponding array of interconnections.

27. The method of claim 26, wherein the solder balls comprise a solder shell surrounding a solid center of a material having a higher melting temperature than the solder shell.

28. The method of claim 27, wherein the solder shell is made of a lead-free solder and the solid center is copper or aluminum.

29. The method of claim 26, wherein the component is an electronic component housed in a ball grid array (BGA) package having a BGA pitch of 0.8 mm or less.

30. The method of claim 29, wherein the component is a land grid array (LGA) socket.